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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,221	12/31/2003	Sang Woon Suh	2950-0281P	7152

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EXAMINER	
YOUNG, BRIAN K	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 12/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,221	SUH ET AL.	
	Examiner	Art Unit	
	Brian Young	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/31/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

2. Claims 1-11 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-11 of prior U.S. Patent No. 6,696,994. This is a double patenting rejection.

The claims appear to be exactly the same as the previously allowed claims in the parent application.

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Isomura discloses a data encoding method of a multiple-valued information source includes a prediction setting process defining either "0" or "1" as a superior symbol and the other as an inferior symbol, when a multiple-valued information source that includes a plurality of bits is divided into bit planes and a binary bit string that includes "0"s and "1"s of each bit plane is input, predicting the superior symbol to continue for n units, and setting that n units as a prediction bit number; and a prediction result output process outputting either signal of "0" or "1" as a prediction correct signal, being a code word, when prediction is correct for an observed series composed of the above-mentioned prediction bit number input, and moving to the operation of encoding

the next string of n bits, and outputting the other of either "1" or "1" as a prediction failed signal, as a code word, when the prediction has failed in the encoding operation; wherein a similar prediction setting process and prediction result output process are recursively iterated, setting a newly-decreased prediction bit number as a prediction bit number less than n units when the prediction has failed a specified number of times.

When a multiple-valued information source is divided into bit planes and the superior symbol of each bit plane is predicted to continue for n units, and when the prediction was correct, the n bits become represented by a single prediction correct signal, and the speed of encoding is increased in addition to increasing the efficiency of compression. Moreover, when the prediction has failed because reducing the number of prediction bits performs the next prediction, the efficiency of compression and speed of encoding is not reduced very much, even when the prediction fails.

Laury et al disclose an image processing circuit adapted to replace an input code associated with a pixel of the image with an output code selected in first storage means containing a set of codes, which includes an input bus adapted to receive the input code, an output bus adapted to provide the output code, said first storage means, means of address calculation of the first storage means, means of address selection of the first storage means between the input code and an address code generated by the address calculation means, second storage means adapted to contain an address code generated by the address calculation means, and means of selection of the output code between a code read at the current address of the first storage means and said code

contained in the second storage means.

The address calculation means include an address generator adapted to provide predetermined address codes to the addressing means, and a data comparison circuit provided to compare the first code with the codes stored at the predetermined addresses in the first storage means, to determine which of the compared codes is closest to the first code, and to control the second storage means to store the code of the address at which the closest compared code is stored in the first storage means.

The input and output buses each include first, second, third, and fourth sub-buses each having a same number of bits, the address selection means include first, second, third, and fourth multiplexers, the first inputs of which are respectively connected to the first, second, third, and fourth input sub-buses, the output of the first multiplexer being connected to the second inputs of the second, third, and fourth multiplexers, the first storage means include a first, a second, a third, and a fourth identical memory circuits, the addressing inputs of which are respectively connected to the outputs of the first, second, third, and fourth multiplexers, and the output code selection means include a fifth multiplexer, the first input of which is connected to the data output of the first memory circuit and the output of which is connected to the first output sub-bus, the second, third, and fourth sub-buses being respectively connected to the data outputs of the second, third, and fourth memory circuits.

Kumamaru (JP401181214A) discloses three components of a data series generator

10, an interpolation estimate device 20 and an average value calculator 30, eliminates noise component as to an inputted data string S<SB>1</SB> and outputs the result as a data row S<SB>0</SB>. The data series generator 10 extracts data from the inputted data row S<SB>1</SB> at an interval of n-set of data and outputs n-set of data rows D<SB>1</SB>∼D<SB>n</SB>. In this case, the (n-1)-set of data are missing. The interpolation estimate device 20 interpolates missing data and outputs data strings E<SB>1</SB>∼E<SB>n</SB> after the interpolation. The average value calculator 30 arranges the data series after interpolation on the same time axis respectively, obtains a mean value of each data on the same position of the time axis and outputs a series of data rows comprising the obtained mean value as the data string S<SB>0</SB>.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Young
Primary Examiner
Art Unit 2819

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